In the specification

Please replace the last paragraph at page 1, starting with the word "This" with the following paragraph:

--This problem with the prior art method is illustrated in more detail in Fig. 2(a), Fig. 2(b), and Fig. 2(c). As shown in Fig. 2(a), a resist layer 11, a $5i0_2$ layer 12 and a Cu interconnect layer 13 are formed at a first step, and a via hole 17 extending to the copper interconnect layer 13 is formed at the second step.--

Please rewrite two paragraphs at page 2, lines 2-8 as follows:

--At this step, copper on the surface of the copper interconnect layer acts on the via hole side surface so as to form a copper deposition 14 on the side surface, this side surface copper deposition being a cause of leakage current.

In addition. there is oxidation 15 of the copper surface of the copper interconnect layer, this oxidation leading to an increase in electrical resistance. The barrier performance of a TaN barrier film 16 formed as shown in Fig. 2(c) is weak in the barrier characteristic.--

Please rewrite the paragraph at page 4, lines 9-19 as follows:

--A first aspect of the present invention is a semiconductor device which comprises, a substrate, on a main surface of which, interconnect layers made at least of copper are formed along with a predetermined pattern in buried condition. an etching-stop layer formed on the main surface of the substrate, and an insulation layer formed on the etching-stop layer, and wherein the semiconductor device further comprises a via-hole provided on a main surface of the insulation layer and penetrating through the insulation layer and the etching-stop layer so that a bottom of the via hole reaches at a surface of the